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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Application Number	10/551,837
		Filing Date	October 3, 2005
		First Named Inventor	Soha M.N. Hassoun
		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
Sheet 2 of 2	Attorney Docket Number	TUFTS-002AUS	

OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
BH		PCT/US2004/010320 International Search Report dated October 4, 2004.	
BH		W. ROBERTSON, S. PERIYALWAR, W. J. PHILLIPS, RTL Synthesis for Systolic Arrays, Proceedings of the International Symposium on Circuits and Systems, May 3-6, 1993, Volume 2, New York, IEEE, US.	
BH		M'ODRAG PTOKONJAK, WAYNE WOLF, Cost Optimization in ASIC Implementation of Period Hard-Real Time Systems Using Behavioral Synthesis Techniques, November 5-9, 1995, pp. IEE/ACM International Conference on Computer-Aided Design, IEE Comp. Soc. Press, US	
BH		U. NAGARAJ SHENOY, PRITH BANERJEE, ALOK CHOUDHARY, A System-Level Synthesis Algorithm with Guaranteed Solution Quality, March 27, 2000, Pages 417-424, Paris, France.	

Examiner Signature		Date Considered	11/07/07
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.  
<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.  
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